Group 1

1. Write the Eber-Moll equation on normal operation and inverted operating using superposition of two currents.
2. Define saturated, non-saturated, and uni-polar logic family and give examples of it.
3. Why monostable multivibrator is called as on shot multivibrator?
4. Analyze the Diode Transistor Logic (DTL) circuit with input low.
5. Draws the two inputs DTL AND-OR-INVERT gates circuits and DTL NOR gate circuit.
6. Determine the one input is low for TTL circuit model.
7. Discuss the NMOS inverter with resister load at cut off and non-saturation region.
8. Discuss the NMOS inverter with resister load at non-saturation and transition region.
9. Show that, n-channel MOSFET with depletion load is differing from others.
10. Explain the driver transistor curve and load curve of the NMOS.
11. Analyze the CMOS inverter for V_I is just greater than V_{TN} when both transistors are enhancement mode devices.
12. Give complete voltage transfer characteristics of the CMOS inverter when both transistors are enhancement mode devices.
13. Construct the two inputs CMOS NAND gate with its truth table.
14. How ROM is differs from RAM? Give its importance and examples also.
15. Write down the importance of photolithography process in IC fabrication.
16. Realize the PLA and make PLA tables for the following logic expressions:

    $F0 = \sum m (0, 8, 15, 12, 5, 7, 3)$
    $F1 = \sum m (2, 5, 6, 8, 10, 13, 15)$
    $F3 = \sum m (1, 4, 5, 7, 9, 12, 15)$
    $F4 = \sum m (5, 6, 8, 10, 11)$
17. Write short notes.
    a. Charge Coupled Devices
    b. SDRAM
    c. Bistable multivibrator
    d. Power dissipation in CMOS inverter
    e. NMOS transmission gate

Roll No.: 01 to 10

Group 2

1. Why the Eber-Moll model is called ‘T’ model? Describe charge distribution in the base.
2. What are the parameters to characterize digital ICs, how can you compare performance of it.
3. Write operation procedures for monostable multivibrator when it is in stable state.
4. Calculate maximum low input voltage for DTL circuit, when supply voltage is 5 volts and take the appropriate values of resisters.
5. Explain the operation of DTL logic circuit.
6. Explain the operation of TTL logic circuit when all inputs high.
7. Write down the three formulae used in n-channel MOSFET.
8. What are the basic properties of logic gates? Write down, MOSFET inverters with resistive load.
9. Justify all possible cases for voltage input and output characteristics for NMOS inverter with depletion load.
10. What are the differences in the concept of effective width to length ratios of NMOS logic circuit?
11. Analyze the CMOS inverter for $V_I = V_{DD}$ when both transistors are enhancement mode devices.
12. Give the possible logics for CMOS inverter design consideration.
13. Write FAN-IN and FAN-OUT of CMOS inverter.
14. Write operation procedures for SRAM.
15. Realize the PLA and make PLA tables for the following logic expressions:

    $F0 = \sum m (0, 8, 15, 12, 5, 7, 3)$
    $F1 = \sum m (2, 5, 6, 8, 10, 13, 15)$
    $F3 = \sum m (1, 4, 5, 7, 9, 12, 15)$
    $F4 = \sum m (5, 6, 8, 10, 11)$
16. What are the main steps follow during IC fabrication?
17. Write short notes.
    a. Noise Margin
    b. Charge Coupled Devices
    c. Power dissipation in CMOS inverter
    d. NMOS transmission gate
    e. Comparison between BJT and MOS

Roll No.: 11 to 20

Group 3

1. Write the Eber-Moll equation on normal operation and inverted operating using superposition of the four currents.
2. What is multivibrator? Explain the Bistable multivibrator briefly.
3. Write operation procedures for monostable multivibrator when it is triggered.
4. Describe the operation procedures when Resister Transistor Logic input high with circuit diagram.
5. How Transistor Transistor Logic (TTL) is differing from DTL?
6. Explain the operation of ECL logic circuit.
7. How NMOS is replaced by CMOS? Justify.
8. Explain input and output voltage characteristics curve for NMOS inverter with resister load.
9. What will happen when i) $V_I < V_{TND}$, ii) V_I is just greater than V_{TND}, iii) transition point for the driver, NMOS inverter with depletion load?
10. Define NMOS NOR logic gate with depletion load and realize the all possible combinations for two inputs.
11. Analyze the CMOS inverter for $V_I = 0$ when both transistors are enhancement mode devices.
12. Generalized CMOS inverter current when NMOS inverter biased in the saturation region.
13. What are the most important parameters for evaluating and comparing logic families?
14. What are the differences between SRAM and DRAM? Give its symbolic representation.
15. How can you say that 555 Timer IC is most popular commercially available integrate-circuit packages? Give the internal function diagram of the 555IC.
16. Realize the PLA and make PLA tables for the following logic expressions:

    $F0 = \sum m (0, 8, 15, 12, 5, 7, 3)$
    $F1 = \sum m (2, 5, 6, 8, 10, 13, 15)$
    $F3 = \sum m (1, 4, 5, 7, 9, 12, 15)$
    $F4 = \sum m (5, 6, 8, 10, 11)$

17, Write short notes.
    a. A 3-bit CCD shift register
    b. Basic steps of IC fabrication
    c. Enhanced DRAM
    d. Difference between NMOS and PMOS
    e. CMOS transmission gate

Roll No.: 21 to 30

Group 4

1. What are the delay, rise, storage, and fall time for BJT switching? Explain each with neat diagrams.
2. Why astable multivibrator is called as free running multivibrator? Justify.
3. What are the advantages and limitations of resister transistor logic?
4. Analyze the Diode Transistor Logic (DTL) circuit with all input high. Calculate the maximum load current.
5. Explain the operation of TTL logic circuit.
6. What are the merits, demerits, and uses of ECL?
7. How merge transistor logic is differing from other logic family?
8. Write down the current voltage relationship for NMOS inverter with resister load.
9. What is the advantage of depletion load inverter over the enhancement load inverter?
10. Define NMOS NAND logic gate with depletion load and realize the all possible combinations for two inputs.
11. Write down the CMOS properties, and draw cross section view of CMOS logic.
12. Generalized CMOS inverter current when PMOS inverter biased in the saturation region.
13. Analyze the CMOS transmission gate when i. input high condition, ii. Input low condition, iii. Remains in dynamic condition.
14. Give the RAM family chart. How main memory differ from the mass storage memory.
15. Design a programmable logic array (PLA) using AND matrix and OR matrix, which should realize the following logic expressions:

    Y0 = mn'o + m'no + m'no' + mn'o'
    Y1 = mno' + m'n'o + m'no'
    Y2 = m'n'o + mn'o + mn'o'
    Y3 = mno + mn'o' + m'no'

16. What are the ten basic steps of photolithography process during semiconductor fabrication process?

17, Write short notes.

    a. Difference between NMOS and PMOS
    b. Power dissipation in CMOS inverter
    c. NMOS transmission gate
    d. Enhanced DRAMs
    e. Comparison between BJT and MOS

Roll No.: 31 to 39

Group 5

1. How can you improve BJT time? Give circuit diagram and corresponding wave form.
2. Write operation procedures for astable multivibrator.
3. Derive the operation procedures when Resister Transistor Logic input both low to both transistor with circuit diagram.
4. Draw the two input DTL AND gate circuits and DTL OR gate circuit.
5. Determine the maximum low input current for TTL circuit model.
6. Explain the operation of ECL 10K series with circuit diagram.
7. What are the important features of Integrated Injection Logic (IIL)? Draw the circuit diagram of 2 input IIL circuit.
8. What are the major differences between NMOS inverter with resister load and enhancement load? Which NMOS inverter is greater in size and how?
9. What are the difference between NMOS and PMOS?
10. How can you say that rise time is relatively longer than fall time of an NMOS inverter with depletion load? Justify.
11. What are the merits of CMOS logic? Explain the operations of this logic.
12. Construct the two inputs CMOS NOR gate with its truth table.
13. How can you design CMOS NOR symmetrical gate?
14. Explain the semiconductor memories with its basic properties.
15. Design a programmable logic array (PLA) using NMOS, which should realize the following logic expressions:

    $F0 = \sum m (0, 8, 15, 12, 5, 7, 3)$
    $F1 = \sum m (2, 5, 6, 8, 10, 13, 15)$
    $F3 = \sum m (1, 4, 5, 7, 9, 12, 15)$
    $F4 = \sum m (5, 6, 8, 10, 11)$
16. What are the ten basic steps of photolithography process during semiconductor fabrication process?
17. Write short notes.
    1. Propagation Delay Time
    2. Charge Coupled Devices
    3. Enhanced DRAM
    4. Difference between NMOS and PMOS
    5. Comparison between BJT and MOS

Roll No.: 40 to 48