Programme Specifications

Programme: M. Tech. in VLSI and Nanotechnology	
Faculty	Faculty of Engineering and Technology
Department	Electronics and Communication Engineering
Programme	M.Tech in VLSI and Nanotechnology
Dean of Faculty	Dr. M. Arulanantham
HOD	Dr. Raghavendra V. Kulkarni

1.	**Title of the Award**
	M. Tech. in VLSI and Nanotechnology
2.	**Modes of study**
	Full Time and Part Time
3.	**Awarding Institution / Body**
	M. S. Ramaiah University of Applied Sciences – Bengaluru, India
4.	**Joint Award**
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5.	**Teaching Institution**
	Faculty of Engineering & Technology
	M S Ramaiah University of Applied Sciences - Bengaluru, India
6.	**Date of Programme Specification**
	24-Jul-2019
7.	**Date of Programme Approval by the Academic Council of MSRUAS**
	24-Jul-2019
8.	**Next Review Date**
	01-May-2021
9.	**Programme Approving Regulatory Body and Date of Approval**
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10.	**Programme Accrediting Body and Date of Accreditation**
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11.	**Grade Awarded by the Accreditation Body**
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12.	**Programme Accreditation Validity**
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13.	**Programme Benchmark**
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14. Rationale for the Programme	
	Very Large-Scale Integration (VLSI) system design is the process of creating complex integrated circuits by combining million/billion number of transistors into a single chip. This programme aims to prepare the students to design analog and digital integrated circuits using custom and semicustom design flow. Worldwide, for the past five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The improvement of integration level, cost, speed, power, compactness and functionality of the integrated circuits leads to significant improvement in economic productivity and overall quality of life through proliferation of computers, communication, industrial and consumer electronics. In India, being a fast-changing technology area, VLSI design is an extremely challenging and creative sector that offers exciting opportunities and fast growth for engineers. Bangalore is often referred to as the Silicon Valley of India. The growing number of product and service-based semiconductor industry, thus various career opportunities exist in product development companies of VLSI that includes mobile and consumer electronics, computing, telecommunications, networking, data processing, automotive, healthcare and industrial applications. The improvement and complexity of VLSI system can be achieved by revolution of CMOS transistors, miniaturization of transistors, VLSI design methodology, EDA tool support, fabrication support, new design idea and innovative technology which are active research area in VLSI system design. The scaling of devices is making integration of large number of devices in a single chip possible. But there is a limit to this scaling. At some point of time there has to be a switch from traditional semiconductor devices to newer and hybrid Nano devices like carbon nanotubes and tunneling devices like single electron transistors, quantum dots, and tunneling diodes. The future prospects Nanotechnology are great, because it will involve research in various fields like quantum mechanics, material science, device modelling and development, circuit design fabrication and testing. To sustain the growth rate of semiconductor industry, industries are in need of designers, analysts, developers, testing and marketing engineers as well as managers with a postgraduate degree. The demand for VLSI design engineers as well as research in Nano electronics are constantly growing in India. Through this programme of M.Tech in VLSI and Nanotechnology, MSRUAS will able to support the expected demand.

15. Programme Aim

The aim of the course is to produce postgraduates with advanced knowledge and understanding of VLSI system design and Nanotechnology; higher order critical, analytical, problem solving and transferable skills; ability to think rigorously and independently to meet higher level expectations of VLSI industry, academics, Nano electronics research or take up entrepreneurial route.

16. Programme Objectives

The objectives of the programme are to enable the students to:

1. Establish a foundation of working principles of nanoscale devices and their design theories of next generation circuits and systems.
2. Develop the ability to model, design, analyze, simulate, verify and implement analog/ digital circuits and systems both at chip level and board level.
3. Educate in embedded programming using HDL and design methodology for the development of FPGA based embedded system.
4. Educate in the characterization of Micro and Nano electronic devices and circuits for implementing efficient systems using top-down and bottom up approach.
5. Promote teamwork, lifelong learning and continuous improvement.

17. Intended Learning Outcomes of the Programme

The Intended Learning Outcomes (ILOs) are listed under four headings:
1. Knowledge and Understanding, 2. Cognitive Skills 3. Practical Skills and 4. Capability / Transferable Skills.

1. Knowledge and Understanding

After undergoing this programme, a student will be able to:

KU1: Discuss the working principles of analog, digital and mixed signal circuits

KU2: Explain the use of FPGA in ASIC design and embedded system development

KU3: Explain the concepts of quantum mechanics of atoms and molecules, properties of nanomaterials and voltage -current characteristics of nanoscale devices

KU4: Describe the latest developments in VLSI system design style, integration technology and fabrication of Nano devices from Nano materials

2. Cognitive Skills

After undergoing this programme, a student will be able to:

CS1: Analyze the CMOS circuits and optimize it for enhancing the performance of integrated circuits

CS2: Use quantum mechanics concepts and apply for quantum communication and computing

CS3: Design and analyze FPGA-SoC architectures for various embedded applications including IoT

CS4: Design new Nano devices and circuits with high performance and low power conception

3. Practical Skills

After undergoing this programme, a student will be able to:

PS1: Use EDA tools to model, design, develop and analyze, CMOS integrated circuits

PS2: Use EDA tools to develop to prototype applications on FPGA

PS3: Use standard software tools to understand and analyze the working of Nano devices at molecular level

PS4: Use EDA tool to verify and validate integrated circuits, FPGA-SoC systems

4. Capability / Transferable Skills

After undergoing this programme, a student will be able to:

TS1: Manage information, develop technical reports and make presentations

TS2: Build, Manage and Lead a team to successfully complete a project and communicate across teams and organizations to achieve professional objectives

TS3: Work under various constraints to meet project targets

TS4: Adopt to the chosen profession by continuously upgrading his/her knowledge and understanding through Life-long Learning philosophy

18. Programme Structure

The Programme consists of four terms as shown below. A student is required to successfully complete the following courses and earn credits for the award of the degree.
Complete details of each of the courses such as ILO's, content, resources, teaching-learning processes and other related information are outlined in Course Specification of the respective programme.

SEMESTER 1

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLC501A	Full Custom IC Design	3	0	2	4	100
2	19VLC502A	Quantum Mechanics and Nano Electronics	2	1	2	4	100
3	19VLC503A	Semi-Custom IC design	3	0	2	4	100
4	19VLC504A	Nano Scale Device Modelling and Simulation	2	1	2	4	100
5	19VLE51XA	Refer to Elective Course Table	3	0	2	4	100
6	19FET508A	Research Methodology & IPR	2	--	--	2	50
7	19FET509A	Professional Communication	1	--	--	0	00
		Total	**16**	**2**	**10**	**22**	**550**
	Total number of contact hours per week		**28 hours**				
	Number of credits can be registered		**Minimum**	**18**		**Maximum**	**24**

SEMESTER 2

Sl No	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLC511A	FPGA System Design and Implementation	3	0	2	5	100
2	19VLC512A	Nano Materials and Devices	3	0	2	5	100
4	19VLE52XA	Refer to Elective Course Table / MOOC	4	0	0	4	100
5	19VLE52XA	Refer to Elective Course Table / MOOC	4	0	0	4	100
6	19VLE52XA	Refer to Elective Course Table / MOOC	4	0	0	4	100
9	19FET510A	Value Education	1			0	
		Total	**19**	**0**	**4**	**22**	**600**
Total number of contact hours per week			**23 hours**				
Number of credits can be registered			**Minimum**	**18**		**Maximum**	**24**

SEMESTER 3

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLP521A	Internship/other activities			10	4	100
2	19VLP522A	Group project			15	8	200
3	19VLP523A	Dissertation and Publication (Phase 1)					
Total					**25**	**12**	**300**
Total number of contact hours per week			**25 hours**				

SEMESTER 4

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLP523A	Dissertation and Publication (Phase 2)			24	24	400
Total					**24**	**24**	**400**
Total number of contact hours per week			**24 hours**				

Elective Course List				
Stream / Specialization	**S. No.**	**Course Code**	**Course Title**	**Course Category**
VLSI	E11	19VLE511A	Signal Integrity and High-Speed Design	A
	E12	19VLE512A	VLSI Verification and Testing	B
	E13	19VLE513A	Analog and Mixed Signal Circuit Design	B
	E14	19VLE514A	Programmable Embedded SoCs	B
Nanotechnology	E21	19VLE521A	Sensors and Systems Design	A
	E22	19VLE522A	MEMS and NEMS	B
	E23	19VLE523A	Advanced Nano Materials and Applications	B
	E24	19VLE524A	Quantum Computing and Communication	B

Course category	Course classification	Type of course
A	Core/Electives	Theory (T) + Lab (L) combined
B	Core/Electives/ Mandatory	Theory (T) only
C	Mandatory (Compulsory) Modules	Theory (T)
G	Group Project	Team Work
I	Internship/Other activities	Individual work
DP	Dissertation and Publication	Individual work

19. Programme Delivery Structure

A Programme is delivered from Monday to Saturday of the week as per the Time-Table for every batch.

20. Teaching and Learning Methods

The course delivery comprises of a combination of few or all of the following:

1. Face to Face Lectures using Audio-Visuals
2. Workshops, Group Discussions, Debates, Presentations

3. Demonstrations
4. Guest Lectures
5. Laboratory/Field work/Workshop
6. Industry Visit
7. Seminars
8. Group Exercises
9. Project Exhibitions
10. Technical Festivals

21. Courses

Programme has six Professional core courses, four Professional elective courses, two audit courses, and one compulsory course followed by Group Project, Internship and Dissertation & Publication courses.

Core courses are Programme Specialization courses which normally include both theory and laboratory sessions. Alternate activities are planned in case of laboratory sessions do not exist in a course.

Compulsory course is Research Methodology and IPR course which is mandatory.

All courses of the programmes are categorized as indicated in the **Annexure I.**

22. Electives

There are 4 electives in the programme. The electives are grouped such a way that a student can choose a set of electives to specialize in a chosen field/stream. However, if the student wishes to opt for elective course that spans multiple streams, the case may be considered subject to the affordability of academic logistics and approval by the course leader, HODs and Deans.

For every elective offered, there will be a minimum and a maximum number of registrations that is decided by the department.

There is also a provision for the students to choose Electives through on-line mode such as MOOC's, SWAYAM, NPTEL and other equivalent platforms. The guidelines prescribed by the University for such courses to be adhered to. The student can also earn 3 or 4 credits by participating in the international competitions like technical presentation/ conference/ publications in the journal etc and winning the award in that. In that case he/she can be exempted from one of the elective courses of the programme.

23. Group Project

The main objective of group project is to provide an ambiance to work in groups towards achieving a common goal. A group shall have up to 5 students. In case of Group Project work is based on inter-disciplinary in nature, team can be constituted with members from across departments of the Faculty.

The students are required to develop a report for assessment and also need to demonstrate the working of the product. The IPR rights of all such work lies with the University only. The project should be approved by a committee constituted by respective HoDs before the start of the project. For further details related to the Group Project refer to Course Specification of the respective programmes

24. Industry Internship/Other Activities

A student can opt for an internship in an industry, a business or research organization during the course.

Alternately, can undertake a mini-project requiring self-directed study that can be perused within the affiliated Faculty.

Prior approval of the internship / mini-project by the HoD and Dean is mandatory. It is also necessary for the student to submit a report and make a presentation to the members of the panel constituted by the HoD for assessment.

For further details related to this course, please refer to Course Specification of the respective programmes.

25. Dissertation and Publication

This course has two parts – Dissertation and Publication.
Every student, has to undertake the dissertation work individually on a chosen relevant topic. The topic needs to be approved by the committee constituted by HoD.
Publication is a stage wherein dissertation work of the student is converted into a technical paper to be published in reputed conferences/journals.
For further details related to the this course refer to Course Specifications of the respective programmes

26. Course Assessment

a. Every course will be assessed for a weight of 100%

b. For the courses having 100% theory

There are two components-Component-1 and Component-2

Component-1 (CE) carries a weight of 50% and Component -2 (SEE) carries a weight of 50%

Component-1 (CE): 50% weight

The course leader will indicate the mode of assessment in consultation and approval of the respective HoD and the faculty Dean, before commencement of the semester. The template for weightage of CE and SEE in percentages for each theory course is indicated in the Table below.

ILO No.	Intended Learning Outcome	CE (Weightage: 50 %)				SEE
		Assessment Type	Comp-1a	Comp-1b	Comp-1c	(Weightage : 50 %)
		Comp Weightage (%)	00	00	00	Sem End Exam
1	ILO-1					
2	ILO-2					
3	ILO-3					
4	ILO-4					
5	ILO-5					
6	ILO-6					

CE – can be from any combination of the following:

Assignments, term Tests, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, others, if any.

Component - 2 (SEE): 50% weight

A 3 hour duration Semester End Examination will be conducted for a maximum of 100 marks and will be reduced to 50% weight.

A student is required to score a minimum of 40% marks in Semester end examination and 40% marks overall in each theory course.

c. For Laboratory/ Practical courses

Total Marks : 50

Component 1(CE) : Laboratory Report: 50% Weight

Component 2(SEE) Semester End Examination: 50% Weight

A 3 hour duration Semester End Examination will be conducted for a maximum of 50 marks.

The course leader will indicate the mode of assessment in consultation and approval of the respective HoD and the faculty Dean, before commencement of the semester.

The template for weightage of CE and SEE in percentages for each course is indicated in Table below.

ILO No.	Intended Learning Outcome		CE (Weightage: 50 %)				SEE (Weightage: 50 %):
		Assessment Type	Conduction of Lab Exercises)	(Viva)	(Lab Record Submission)	(Lab Test)	SEE
		Comp Weightage (%)					50
1	ILO-1						
2	ILO-2						

A student is required to score a minimum of 40% marks in Semester end examination and

40% marks overall in each laboratory course.

d. **For courses with a combination of theory and laboratory**

There are two components-Component-1 and Component-2

Component-1 (CE) carries a weight of 50% and Component -2 (SEE) carries a weight of 50%.

Component-1 (CE): 50% weight

The course leader will indicate the mode of assessment in consultation and approval of the respective HoD and the faculty Dean, before commencement of the semester. The template for weightage of CE and SEE in percentages for each course is indicated in Table below.

ILO No.	Intended Learning Outcome	CE (Weightage: 50 %)				SEE (Weightage: 50 %)
		Assessment Type	Comp-1a	Comp-1b	Comp-1c Lab	SEE
		Comp Weightage (%)	00	00	00	50
1	ILO-1					
2	ILO-2					
3	ILO-3					
4	ILO-4					
5	ILO-5					
6	ILO-6					

CE – can be from any combination of the following:

Assignments, term Tests, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, others

A 3 hour duration Semester End Examination will be conducted for a maximum of 100 marks and will be reduced to 50 marks.

A student is required to score a minimum of 40% marks in Semester end examination and 40% marks overall in each theory course.

e. Other flexibilities (exceptions) as per the programme regulations.

27. Failure in Course and Makeup Examinations

Makeup Examinations are provided for the students who are not able to meet all pass criteria prescribed for a course during the regular term and fail in the course.
For further details related to makeup examination, please refer to M.Tech. Programme Academic Regulations document.

28. Attendance

Please refer to M.Tech. Programme Academic Regulations document for attendance requirements and condonation related details.

29. Award of Grades

As per the M.Tech. Programme Academic Regulations document.

30. Student Support for Learning

Students are provided with various facilities to support learning such as the following:

1. Course notes
2. Reference books in the library
3. Magazines and Journals
4. Internet facility
5. Computing facility
6. Laboratory facility
7. Workshop facility
8. Staff support
9. Lounges for discussions
10. Any other support that enhances their learning

31. Quality Control Measures

Following are the Quality Control Measures:

1. Review of course notes
2. Review of question papers and assignment questions
3. Student Feedback Analysis
4. Moderation of assessed work
5. Opportunities for the students to see their assessed work
6. Review and audit by external examiners
7. Staff Student Consultative Committee meetings
8. Student exit feedback analysis

32. Curriculum Map

Course Code	Intended Learning Outcomes															
	Knowledge and Understanding				Cognitive (Thinking) Skills (Critical, Analytical, Problem Solving, Innovation)				Practical Skills				Capability / Transferable Skills			
	KU1	KU 2	KU3	KU4	CS1	CS2	CS3	CS4	PS1	PS2	PS3	PS4	TS1	TS2	TS3	TS4
19VLC501A	X			X	X				X							
19VLC502A			X	X		X					X					
19VLC503A	X			X	X				X							
19VLC504A			X	X							X					
19VLE51XA				X		X						X				
19FET508A												X	X	X		
19FET509A												X	X	X		
19VLC511A		X		X			X	X		X	X					
19VLC512A			X	X		X										
19VLE52XA				X								X				
19VLE52XA				X								X				
19VLE52XA		X		X								X				
19FET510A												X	X	X		
19VLP521A	X	X	X	X	X	X	X	X	X	X	X	X				
19VLP522A		X		X	X	X	X	X		X			X	X	X	X
19VLP523A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

33. Capability / Transferable Skills Map

Course Code	Group work	Self -learning	Research Skills	Written Communication Skills	Verbal Communication Skills	Presentation Skills	Behavioral Skills	Information Management	Personal management/ Leadership Skills
19VLC501A		X		X		X	X		
19VLC502A		X		X		X	X		
19VLC503A		X		X		X	X		
19VLC504A		X		X		X	X		
19VLE51XA	X	X		X			X		X
19FET508A	X	X	X	X	X		X	X	X
19FET509A	X	X		X	X		X	X	X
19VLC511A		X		X		X	X		
19VLC512A		X		X		X	X		
19VLE52XA	X	X		X			X		X
19VLE52XA	X	X		X			X		X
19VLE52XA	X	X		X			X		X
19FET510A	X	X		X	X		X	X	X
19VLP521A	X	X	X		X	X	X	X	X
19VLP522A	X	X	X		X	X	X	X	X
19VLP523A	X	X	X		X	X	X	X	X

34. Co-curricular Activities

Students are encouraged to take part in co-curricular activities like seminars, conferences, symposium, paper writing, attending industry exhibitions, project competitions and related activities to enhance their knowledge and network.

35. Cultural and Literary Activities

To remind and ignite the creative endeavors, annual cultural festivals are held and the students are made to plan and organize the activities.

36. Sports and Athletics

Students are encouraged to develop a habit of taking part in outdoor and indoor games on regular basis.