Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Scheme of teaching and examination

M.Tech. (ET&T) in the Department of Electronics & Telecommunication

2nd Semester

S. No	Board of Study	Subject Code	Subject	Period s per Week			Scheme of Examination			Total Marks	Credit L+(T+P) / 2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	ET&T	528211 (28)	Cryptography and Network Security	3	1	-	100	20	20	140	4
2	ET&T	528212 (28)	Embedded System	3	1	-	100	20	20	140	4
3	ET&T	528213 (28)	Broadband Communication	3	1	-	100	20	20	140	4
4	ET&T	528214 (24)	Digital logic with Verilog Design	3	1	-	100	20	20	140	4
5	Refer Table-II		Elective - II	3	1	-	100	20	20	140	4
6	ET&T	528221 (28)	Network Security Lab	-	-	3	75	-	75	150	2
7	ET&T	528222 (28)	Embedded System Lab	-	-	3	75	-	75	150	2
Total				15	5	6	650	100	250	1000	24

L- Lecture T- Tutorial P- Practical ESE- End Semester Exam CT- Class Test
TA- Teacher's Assessment

TABLE –II			
ELECTIVE –II			
S. No	**Board of Study**	**Subject Code**	**Subject**
1	ET & T	528231 (28)	Adaptive Control System
2	ET & T	528232 (28)	Speech Processing
3	ET & T	528233 (28)	Advanced Micro Electronics

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom.**
Subject: **Cryptography and Network Security** **C**ode: 528211 (28)
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted**: 02**

UNIT – I
Symmetric Ciphers :
Block Cipher Principles, The Data Encryption Standard (DES), A DES Example, Strength Of DES, Differential And Linear Cryptanalysis, Block Cipher Design Principles. Basic Concept In Number Theory And Finite Fields: Divisibility And Division Algorithm, The Euclidean Algorithm, Modular Arithmetic, Groups Rings And Fields, Finite Fields of The Form GF(P), Polynomial Arithmetic, Finite Fields of The Form GF(2^n). Advance Encryption Standard: The Origin AES, AES Structure, AES Round Functions, AES Key Expansion, an AES Example, and an AES Implementation.

UNIT – II
Asymmetric Ciphers
Number Theory**:** Prime Numbers, Fermat's And Euler's Theorem, Testing for Primality, The Chinese Remainder Theorem, Discrete Logarithms; Public Key Cryptography and RSA: Principles of Public Key Cryptosystem, the RSA Algorithm.

UNIT – III
Cryptographic Data Integrity Algorithm
Cryptographic Hash Function**:** Applications of Cryptographic Hash Function, Two Simple Hash Functions, Requirements and Security, Hash Functions Based on Cipher Block Chaining, Secure Hash Algorithm (SHA), SHA-3. Message Authentication Codes: Message Authentication Requirements, Message Authentication Functions, Message Authentication Codes, Security of Macs, Macs Based on Hash Function: HMAC. Macs Based on Block Cipher: DAA and CMAC Authenticated Encryption: CCM and GCM, Pseudorandom Number Generation Using Hash Functions and Macs.

UNIT – IV
Network and Internet Security
Transport Level Security**:** Web Security Issues, Secure Sockets Layers (SSL), Transport Layer Security(TLS), HTTPs, Secure Shell(SSH), Wireless Network Security: IEEE802.11 Wireless LAN Overview, IEEE802.11i Wireless LAN Security, Wireless Application Protocol Overview, Wireless Transport Layer Security, WAP End-to-End Security.

UNIT – V
System Security
Intruders**:** Intruders, Intrusion Detection, Password Management. Firewalls: The Need for Firewalls, Firewall Characteristics, Types of Firewalls, Firewall Basing, Firewall Location and Configurations.

Textbooks:
1. William Stallings, "Cryptography and Network Security", 2nd Edition, Prentice hall of India, New Delhi, 1999

Reference Books:
1. Schneier, Bruce "Applied Cryptography" John Wiley.
2. Behrouz A forouzan ,"Cryptography & Network Security".

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom**
Subject: **Embedded System** Code: 528212 (28)
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I
Overview of Embedded System
Embedded Systems, Processor Embedded Into A System, Embedded Software In A System, Design Process In Embedded System, Classification Of Embedded Systems, Real World Interfacing, Introduction to Advanced Architectures, Processor And Memory Organisation, Instruction Level Parallelism, Performance Metrics, Memory Types , Memory Maps And Addresses, Processor Selection , Memory Selection.

UNIT – II
Devices and Communication Buses for Devices Network
Input and Output types, Serial Communication Devices, parallel Devices ports, sophisticated interfacing features in Devices ports, wireless devices, timer and counting devices, watchdog timer, real time clock, networked embedded systems, serial bus communication protocols, parallel bus device protocols, network protocols, wireless and mobile system protocols.

UNIT – III
PIC microcontroller
Architecture ,Memory Organization , Addressing Modes ,Instruction Set ,PIC Programming In Assembly & C ,I/O Port, Data Conversion, RAM & ROM Allocation, Timer Programming, MP-LAB.
Peripherals Of PIC Microcontroller: Timers, Interrupts, I/O Ports- I^2C Bus-A/D Converter, UART, CCP Modules, ADC, DAC And Sensor Interfacing, Flash And EEPROM Memories.

UNIT – IV
ARM controller
Architecture, Memory Organization, Pipeline And Cache Concepts, ARM (32 Bit) Architecture Instruction Set And Assembly Language Programming - ARM Instructions Set And THUMB Instruction Set, Switching Between ARM And THUMB Instructions.

UNIT – V
RTOS & its overview
Real Time Operating System: Task And Task States, Tasks And Data, Concepts Of Semaphores, Shared Data, Inter process Communication, Signal Function, Semaphore Functions, Message Queue Functions, Mailbox Functions, Pipe Functions,Operating System Services, Process Management, Timer Function, Event Function, Memory Management, Device File And IO Subsystems Management, Interrupts Routines In RTOS Environment, basic Design using an RTOS, RTOS Task scheduling models, interrupt latency and response times of the tasks.

Text Book:
1. Raj Kamal "Embedded Systems – Architecture, Programming and Design", Tata McGraw Hill, 2nd Edition, 2008
2. Steve Furbur, "ARM System-on-chip Architecture", 2nd Edition, Pearson Education
3. John B Peatman ,"Design with PIC micro-controllers" , Pearson Education.

References:

1. Z.Navabi, “Embedded Core Design”, TMH 2nd Edition.
2. Wayne Wolf “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.
3. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier
4. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ‘PIC Microcontroller and Embedded Systems using Assembly and C for PIC18’, Pearson Education 2008.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch**: Electronics & Telecom.**
Subject: **Broadband Communication** Code: 528213 (28)
Total Theory Periods: 40 Total Tutorial Periods: 12
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted: 02

Unit 1
Frame Relays
Frame Relay Protocols and Services**:** Background, Frame Mode Protocol Architecture, Frame Mode Call Control, LAPF; Frame Relay Congestion Control: Congestion In Frame Relay Networks Approaches To Congestion Control, Traffic Rate Management, Explicit Congestion Avoidance, Implicit Congestion Control.

Unit 2
ISDN
The Integrated Digital Network, A Conceptual View Of ISDN, ISDN Standards Interface and Functions: Transmission Structure, User Network Interface; ISDN Protocol Architecture, ISDN Connections, Addressing, Interworking.

Unit 3
B-ISDN Services
B-ISDN Standards, Broadband Services, Requirements, Architecture, B-ISDN Protocol Reference Model, B-ISDN Physical Layer, SONET/SDH

Unit 4
ATM
Asynchronous \Transfer Mode, Transmission of ATM Cells, ATM Adaptation Layer, Requirements For ATM Traffic And Congestion Control, ATM Service Categories, ATM Traffic Related Attributes, Traffic Management Framework, Traffic Management ABR Traffic Management.
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Unit 5
Ad Hoc Networks
Mobile Ad Hoc Networking, Characteristics, Routing Approaches, Proactive and Reactive Protocols, Clustering and Hierarchical Routing, Multipath Routing, Security Aware Routing.

Text Book
1. William Stallings “ISDN and Broadband ISDN with Frame Relay and ATM”, Prentice-Hall, 4th Edition
2. S. Basagni & M.Conti, Mobile Ad Hoc Networking, Wesley, 2004.

References Books
1. Kartalapoulos “Understanding SONET/SDH and ATM”, PHI Publication.
2. Gaskin, James E “Broadband Bible”, Wiley.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom**
Subject: **Digital Logic with Verilog Design** Code: **528214 (28)**
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Examination: **100**
Minimum No. of Class Tests to be conducted: **02**

UNIT 1
Introduction to Logic Circuits
Variables and Functions, Synthesis Using AND, OR and NOT Gates, Introduction to CAD Tools, Introduction to Verilog, Implementation Technology: Transistor Switches, CMOS Logic, PLD, Transmission Gates.

UNIT 2
Optimized Implementation of Logic Functions
Strategy for Minimization, Minimization of POS, Multiple Output Circuits, Analysis of Multilevel Circuits.

UNIT 3
Number Representation and Arithmetic Circuits
Positional Number Representation, Addition of Unsigned Numbers, Signed Numbers, Fast Adders, Design of Arithmetic Circuits using CAD Tools, Multiplication.

UNIT 4
Combinational Circuit Building Blocks
Multiplexers, Decoder, Encoder, Code Converters, Arithmetic Comparison Circuits, Verilog for Combinational Circuits, Flip Flops: Master Slave and Edge Triggered D Flip Flops, T-Flip Flop, JK Flip Flop.

UNIT 5
Sequential circuits design
Synchronous Sequential Circuits: Basic Design Steps, State Assignment Problem, Mealy State Model, Specification of Melay FSM Using Verilog; Asynchronous Sequential Circuits: Asynchronous Behaviour, Analysis Of Asynchronous Circuits, Synthesis Of Asynchronous Circuits, State Reduction.

Text book:

1. S. Brown & Z. Vransesic, "Fundamental of digital Logic with Verilog design ", TMH 2nd Edition.
2. Z.Navabi ,"Verilog System Design" McgrawHill 2nd Edition.

Refferences:

1. Verilog primer by J.Bhasker , Pearson education**.**

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom.**
Subject: **Adaptive Control System** Code: **528231 (28)**
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted**: 02**

UNIT – I
Adaptive Internal Model Control:
Internal Model Control (IMC) Schemes: Known Parameters, Adaptive Internal Model Control Schemes, Stability And Robustness Analysis, Ordinary Direct Adaptive Control with Dead Zone, New Robust Direct Adaptive Control, Robust Adaptive Control with Least Prior Knowledge. Adaptive Variable Structure Control: Problem Formulation, the Case of Relative Degree One the Case of Arbitrary Relative Degree

UNIT – II
Indirect Adaptive Periodic Control & Stability:
Adaptive Control Scheme, Adaptive Control Law. Direct Localization Principle, Indirect Localization Principle. Adaptive Nonlinear Control: Adaptive Passivation, Small Gain-Based Adaptive Control.

UNIT – III
Optimal Adaptive Tracking For Nonlinear Systems:
Problem Statement: Adaptive Tracking, Adaptive Tracking And Atclf's, Adaptive Backstepping, Inverse Optimal Adaptive Tracking, Inverse Optimality Via Backstepping, Design For Strict-Feedback Systems, Transient Performance.

UNIT –IV
Adaptive Inverse for Actuator Compensation :
Plants With Actuator Nonlinearities , Parametrized Inverses, State Feedback Design, Output Feedback Inverse Control, Output Feedback Designs, Designs For Multivariable Systems ,Designs For Nonlinear Dynamics. Direct Adaptive Control ,Indirect Adaptive Control.

UNIT -V
Indirect Adaptive Periodic Control:
Adaptive control scheme ,adaptive control law, direct localization principle, indirect localization principle, adaptive passivation ,small signal based adaptive control.

Textbooks:
1. GANG FENG and ROGELIO LOZANO, “Adaptive Control Systems” Newnes publications, New Delhi.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom**
Subject: **Speech Processing** Code: **528232 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I
Digital Models for the Speech Signal
The Process of Speech Production, The Acoustic Theory of Speech Production, Lossless Tube Models, Digital Models for Speech signals: Vocal Tract, Radiation, Excitation and complete model.

UNIT II
Speech Analysis
Short Time Speech Analysis, Time domain parameters: Short Time Average Energy and Magnitude, Short Time Average Zero Crossing Rate, Short Time Autocorrelation Function; Frequency Domain Parameters: Filter Bank Analysis, Short time Fourier analysis, Formant Estimation and Tracking; LPC Analysis ,Ceptral Analysis.

UNIT III
Coding of Speech signals
Quantization, Measures Of Evaluate Speech Quality, Time Domain Waveform Coding, LPC, Spectral (Frequency Domain) Coders, Vocoders, Vector Quantization Coders.

UNIT – IV
Speech Enhancement
Nature of Interfering Sounds, Speech Enhancement Techniques: Spectral Subtraction and Filtering, Harmonic Filtering, Parametric Re-Synthesis; Spectral Subtraction, Filtering and Adaptive Noise Cancellation, Methods Involving Fundamental Frequency Tracking, Enhancement by Re-Synthesis

UNIT – V
AUTOMATIC SPEECH RECOGNITION
Basic Pattern Recognition Approaches, Parametric Representation Of Speech, Evaluating The Similarity Of Speech Patterns, Networks For Speech Recognition, Adapting To Variability In Speech, Language Models, ANN: Training ANNs, Accommodating Timing In ANNs; Expert System Approach To ASR, Commercial Systems.

TEXT BOOKS:
1. L.R Rabiner and S.W. Schafer "Digital Processing Of Speech Signals ". Pearson Education.
2. Douglas O'Shaughnessy "Speech Communications: Human & Machine ", 2nd ed., IEEE Press.

REFERENCES:
1. Thomas F. Quateri, "Discrete Time Speech Signal Processing: Principles and Practice "1st ed., PE.
2. Ben Gold & Nelson Morgan, "Speech & Audio Signal Processing", 1 ed., Wiley.
3. Claudio Becchetti and Lucio Prina Ricotti, "Speech Recognition ", Wiley.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics & Telecom**
Subject: **Advanced Microelectronics** Code : 528233 (28)
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

Unit 1
Digital Integrated Circuits & Systems
Noise Considerations In Logic Families, Digital System Implementation Using Algorithmic State M/C Concepts, Asynchronous And Synchronous Systems, High Speed Adders, Multipliers, FIFOs, And Barrel Shifters.

Unit 2
Advanced Memory Technology and Design-1
Basics of Memory Advanced Semiconductor Memories, Memory Device and Process Technology, Static Random Access Memory Technology.

Unit 3
Advanced Memory Technology and Design-2
High –performance Dynamic random Access Memory, Non volatile memory, Radiation effects, Ferroelectric memory, Flash Memory, Basic Memory Architecture and Cell Structure.
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Unit 4
Low Power Digital CMOS Design-1
Hierarchy Of Limits Of Power, Introduction, Background, Theoretical Limits, Qasi-Adiabatic Microelectronics, Practical Limits, Conclusion, Switching Component Of Power, Short-Circuit Component Of Power, Static Power.

Unit 5
Low Power Digital CMOS Design-2
Embedded Memory Developments, Cache Memory Designs, Cache Architecture Implementation For A DSP, Embedded SRAM/DRAM Designs, Embedded SRAM Macros, A 1T SRAM Macro, A 4T SRAM Macro, Embedded DRAM Macros, Dramasics, A Compiled 100 MHz DRAM Macro, A Dual-Port Interleaved DRAM Architecture Macro, A 1-Ghz Synchronous DRAM Macro, Merged Processor DRAM Architectures, DRAM Processes With Embedded Logic Architectures, A Modular Embedded DRAM Core, Multimedia Accelerator With Embedded DRAM, Intelligent RAM (IRAM),Computational RAM.

TEXT BOOKS:
1. Ashok K. Sharma," Advanced Semiconductor Memories: Architectures, Designs, and Applications ", 2002, Wiley-IEEE Press
2 A.P. Chandrakasan and R Brodersen, Kluwer,"Low Power Digital CMOS Design", Academic Publishers. 1995

REFERENCES:
1. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability", Wiley-IEEE Press, 2002
2. Kaushik Roy and Sharat Parsad ,"Low Power CMOS VLSI Circuit Design" , John Wiley & Sons.1998
3. Charles Mckay ,"Digital Circuits: A Proportion for Microprocessors ",Prentice Hall,1994.
4. John F. Wakherly,"Digital Design: Principle and Practices ", PHI International, 1994.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics &Telecom.**
Subject: **Embedded System Lab** Code: **528222 (28)**
Total Practical Periods: **40**
Total Marks in End Semester Examination: **75**

Experiments to be performed:

1. Write an assembly language program for square wave generation using PIC MC Timers.
2. Write an assembly language program for establishing serial communication using PIC MC serial interrupts.
3. Write an assembly language program for interfacing LCD display unit to PIC MC.
4. Write an assembly language program for interfacing stepper motor to PIC micro controller.
5. Write an assembly language program for interfacing ADC to PIC micro controller.
6. Write an assembly language program for interfacing Matrix Keypad (4x4) to PIC micro controller.
7. Write an assembly language program for performing arithmetic operation on ARM microcontroller.
8. Write an assembly language program for Serial Communication between ARM Development board and PC
9. Write an assembly language program for matrix multiplication on ARM microcontroller.
10. Write an assembly language program for serial communication using ARM microcontroller.
11. Write an assembly language program for interfacing LCD display unit to ARM Processor.
12. Design with ARM Processors: I\O Programming, ADC DAC, Timers, Interrupts

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Semester: **M.Tech. II Sem.** Branch: **Electronics &Telecom.**
Subject: **Network Security Lab** Code: **528221 (28)**
Total Practical Periods: **40**
Total Marks in End Semester Examination: **75**

List of Experiments (To be performed at least 10 Experiment)

1. Design and Simulation of Network / System threats including, Denial of Service (DoS) and Distributed Denial of Service (DDoS).
2. Design and Simulation of Network / System threats including Sniffing – Packet / Mail sniffing.
3. Design and Simulation of Network / System threats including Spoofing – IP, MAC.
4. Simulate Web Vulnerabilities with Web based password capturing, SQL injection (injection discovery, form validations), and Buffer overflow.
5. Design and Simulate Web Vulnerabilities with Honeypots – Active, anti-intrusion technique
6. Simulate System Threat Including, Trojans & Backdoors.
7. Design & Simulate Virus & AV methods.
8. Simulate Network Identification with Enumeration – TCP ping, Ping sweep, ICMP ping, NULL Scan, Fast Scan, UDP port scan, Syn Stealth, Fin Stealth.
9. Design and Simulation of hiding a text in an image.
10. Experiment of Cryptography with Symmetric Encryption Scheme, Stream Cipher – RC4.
11. Experiment of Cryptography with Symmetric Encryption Scheme, Block Cipher – S-DES, 3-DES.
12. Experiment of Cryptography with Asymmetric Encryption Scheme, Block Cipher – RSA.
13. Design and Simulation on Hashing Scheme – MD5
14. Design and Simulate Block Cipher Modes – ECB, CBC, CFB, OFB.
15. Study of Authentication Schemes – Different Authentication Schemes Including Password Based Authentication, IP Based Authentication and Challenge Handshake Authentication Protocol (CHAP).