Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Scheme of teaching and examination

M.Tech. (ET&T) in the Department of Electronics & Telecommunication

1st Semester

S. No	Board of Study	Subject Code	Subject	Period s per Week			Scheme of Examination			Total Marks	Credit L+(T+P) / 2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	ET&T	528111 (28)	Modern Digital Communication Technique	3	1	-	100	20	20	140	4
2	ET&T	528112 (28)	Advanced 4G Wireless Network	3	1	-	100	20	20	140	4
3	ET&T	528113 (28)	VLSI System Design	3	1	-	100	20	20	140	4
4	ET&T	528114 (28)	Antenna Theory & Design	3	1	-	100	20	20	140	4
5	***Refer Table – I***		***Elective –I***	3	1	-	100	20	20	140	4
6	ET&T	528121 (28)	Modern Digital Communication Techniques Lab	-	-	3	75	-	75	150	2
7	ET&T	528122 (28)	Simulation with VHDL	-	-	3	75	-	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L- Lecture T- Tutorial P- Practical ESE- End Semester Exam CT- Class Test

TA- Teacher's Assessment

TABLE –I

ELECTIVE -I

S. No	Board of Study	Subject Code	Subject
1	Electrical Engg.	528131 (28)	DSP Processors
2	Electrical Engg.	528132 (28)	RF Circuit Design for Wireless Communication
3	Electrical Engg.	528133 (28)	Neural Network and Application

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M. Tech. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Modern Digital Communication Techniques** Code: 528111 (28)
Total Theory Periods**: 40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted: **02**

Unit 1
Baseband Demodulation /Detection
Signal and Noise, Detection of Binary Signals in Gaussian Noise, Inter Symbol Interference, Equalization.

Unit 2
Communication Link Analysis
The Channel**,** Received Signal Power And Noise Power, Link Budget Analysis, Noise Figure, Noise Temperature & System Temperature, Sample Link Analysis, Satellite Repeaters, System Trade-Offs.

Unit 3
Channel Coding
Reed –Solomon Codes, Interleaving and Concatenated Codes, Coding and Interleaving Applied to the Compact Disc Digital Audio System, Turbo Codes.

Unit 4
Fading Channels
Characterizing Mobile Radio Propagation, Signal Time Spreading, Time Variance of the Channel Caused By Motion, Mitigating the Degradation Effect of Fading, Parameters Characterizing Fading Channels, Applications.

Unit 5
Orthogonal Frequency Division Multiplexing (OFDM)
General Principles**,** Implementation & Signal Processing Aspects For OFDM, Synchronization & Channel Estimation Aspects For OFDM Systems, Interleaving & Channel Diversity For OFDM Systems, Modulation & Channel Coding For OFDM.

Text Books
1 Bernard Sklar ,"Digital Communications", Pearson Publications, 2nd Edition.
2 Henrik Schulze, Christian Luders, "Theory and Applications of OFDM and CDMA", John Wiley & Sons.

Reference Books
1. Wayne Tomasi, "Advanced Electronic Communication Systems", 4th Edition, Oxford University Press, 1998.
2. B.P. Lathi, "Modern Digital and Analog Communication Systems" 3rd edition Oxford University Press, 1998.
3.Ahmad R S Bahai, Burton R Saltzberg ,Mustafa Ergen, "Multi-carrier Digital Communications: Theory and Applications of OFDM." Springer Publications.
4. Marvin K. Simon, Mohamed-Slim Alouini "Digital Communications over Fading Channel" 2nd Edition, A John wiley & Sons, Inc., Publications.
5. Simon Haykin, "Digital Communications" , John Wiley and sons , 1998.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Advanced 4G Wireless Network** Code: 528112 (28)
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. **100**
Minimum number of class test to be conducted: **02**

Unit 1
Introduction of 4G
4G Networks and Composite Radio Environment, Protocol Boosters, Hybrid 4G Wireless Network Protocols.

Unit 2
Physical Layer and Multiple Accesses
Advanced Time Division Multiple Access-ATDMA, Code Division Multiple Access, Multicarrier CDMA, Ultra Wide Band Signal, MIMO Channels and Space Time Coding.

Unit 3
Channel Modeling for 4G
Macrocellular Environments (1.8 GHz), Urban Spatal Radio Channels in Macro/MicroCell Environment (2.154 GHz), MIMO Channels in Micro and PicoCell Environment (1.71/2.05 GHz), Outdoor Mobile Channel (5.3 GHz), Microcell Channel (8.45 GHz), Wireless MIMO LAN Environments (5.2 GHz). UWB Channel Model, Indoor Mobile Channel.

Unit 4
Adaptive and Reconfigurable Link Layer
Link Layer Capacity of Adaptive Air Interfaces, Adaptive Transmission in *Ad Hoc* Networks, Adaptive Hybrid ARQ Schemes for Wireless Links, Stochastic Learning Link Layer Protocol, Infrared Link Access Protocol.

Unit 5
Mobility Management
Introduction, Cellular Systems with Prioritized Handoff, Cell Residing Time Distribution, Mobility Prediction in Pico- and Microcellular Networks.

Text Books
1. Savo G. Glisic" Advanced Wireless Networks 4G Technologies" John Wiley & Sons Ltd.2006.

Reference Books
1. David Tse and Pramod Viswanath , "Fundamentals of Wireless Communications", Cambridge University Press.
2. Andrea Goldsmith" Wireless Communications", Cambridge University Press.
3. Ezio Biglieri "MIMO Wireless Communications", Cambridge University Press.
4. Singhal Bridgman "The Wireless Application Protocol". Pearson Education,2004.
5. T.S. Rappport, "Wireless Digital Communication: Principles and Practices" PHI 1996.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I Sem.** Branch: **Electronics & Telecom.**
Subject: **VLSI System Design** Code**: 528113 (28)**
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Examination: **100**
Minimum No. of Class Tests to be conducted: **02**

UNIT 1
VLSI System Design methodology
Structure Design, Strategy, Hierarchy, Regularity, Modularity, and Locality. System on Chip Design Options: Programmable logic and structures, Programmable Interconnect, Programmable gate arrays; Sea of gate and gate array design, standard cell design, full custom mask design.

UNIT 2
Chip Design Methods
Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System.
Design capture tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

UNIT 3
Data Path Sub System Design
Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations, Array Subsystem Design**:** SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays, Control Unit Design**:** Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.

UNIT 4
Circuit Characterization and Combinational Circuit Design: Delay Estimation: RC Delay Model, Logic Effort, Parasitic Delay, Logic Effort and Transistor Sizing: Delay in Logic, Delay in Multistage Logic Network, Choosing the best Number; Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic ,Dynamic Circuits ,Pass transistor Circuits.

UNIT 5
Introduction To VHDL
Digital System Design Process ,Hardware Simulation , Levels Of Abstraction , VHDL Requirements , Elements Of VHDL , Top Down Design VHDL Operators , Timing , Concurrency , Objects And Classes , Signal Assignments , Concurrent And Sequential Assignments,Structural, Data Flow & Behavioral Description Of Hardware In VHDL**:** Parts Library , Wiring Of Primitives , Wiring Of Iterative Networks , Modeling A Test Bench , Top Down Wiring Components ,Subprograms, Multiplexing And Data Selection , State Machine Descriptions ,Open Collector Gates ,Three State Bussing, Process Statement , Assertion Statement ,Sequential Wait Statements ,Formatted ASCII I/O Operations MSI Based Design.

Text Books :
1. N.H.E.Weste and K.Eshraghian, “Principles of CMOS VLSI Design”, 2nd Edition Addison Wesley, 1993.
2. Jan .M.Rabaey, “Digital Integrated Circuits a design perspective”, PHI 1st Edition, 1995.

Reference:
1. M. Bolton, “Digital System Design with Programmable Logic”, Addison Wesley, 1990.
2. Thomas E. Dillinger, “VLSI Engineering”, Prentice Hall, 1st Edition, 1998.
3. Douglas Perry, “VHDL”, 3rd Edition, McGraw Hill 2001.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I SEM.**
Subject: **Antenna Theory & Design**
Total Theory Periods: **40**
Total Marks in End Semester Examination: **100**
Minimum No. of Class Tests to be conducted: **02**

Branch: **Electronics & Telecom.**
Code**: 528114 (28)**
Total Tutorial Periods: **12**

Unit 1
Antenna Fundamentals
Overview Of The History Of Communications, Significant Contributions To The Understanding Of Electromagnetic Waves, Fundamentals Of Electromagnetic, Solutions Of Maxwell's Equations For Radiation Problems, Ideal Dipole, Radiation Patterns, Directivity And Gain, Antenna Impedance, Radiation Efficiency, Antenna Polarization.

Unit 2
Wire and Broadband Antennas
Dipole Antennas, Folded Dipole Antennas, Yagi-Uda Antennas, Feeding Wire Antennas, Loaded Wire Antennas.Broad Band Antennas: Introduction, Travelling - Wave Antennas, Helical Antennas, Biconical Antennas, Sleeve Antennas, Principles of Frequency - Independent Antennas, Spiral Antennas, and Log Periodic Antennas.

Unit 3
Array Antennas
Introduction, Array Factor For Linear Arrays, Uniformly Excited Equally Spaced Linear Arrays, Complete Array Pattern And Pattern Multiplication, Directivity Of Uniformly Excited, Equally Spaced Linear Arrays, Non Uniformly Excited, Equally Spaced Linear Arrays, Mutual Coupling Arrays, Multidimensional Arrays, Phased Array And Array Feeding Techniques, Elements of Arrays, Wideband Phased Arrays.

Unit 4
Aperture Antennas
Radiation From Apertures And Huygen's Principle, Rectangular Apertures, Techniques For Evaluating Gain, Rectangular Horn Antennas, Circular Apertures, Reflector Antennas , Feed Antennas For Reflectors, Lens Antennas.

Unit 5
Antenna Synthesis
Antenna Synthesis problem, line sources shaped beam synthesis, linear array shaped beam synthesis, low side lobe narrow main beam synthesis methods, iterative sampling method.

Text Books
1. Stutz man and Thiele, "Antenna Theory and Design", 3rdEd, John Wiley and Sons Inc.

Reference Books
1. Kraus, "Antennas", McGraw Hill, TMH, 3" Edition, 2003
2. Kraus and R.J. Marhefka, "Antennas", McGraw Hil1, 2nd Edition, 1998
3. Lo and Hill ," Antenna Handbook "Vol I to IV .
4. C. A. Balanis: "Antenna Theory Analysis and Design", John Wiley, 2nd Edition, 1997

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I Sem.** Branch: **Electronics & Telecom.**
Subject: **DSP Processor** Code: 528131 (28)
Total Theory Periods**: 40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted: **02**

Unit 1
Fundamentals of DSPs Processor
Multiplier And Multiplier Accumulator, Modified Bus Structures And Memory Access In P-DSPs, Multiple Access Memory, VLIW Architecture, Pipelining, RISC And CISC Architecture, Von Neumann And Harvard Architecture, Modified Harvard Architecture, On Chip Peripherals, Computational Accuracy In DSP Processor.

Unit 2
Computational Accuracy in DSP Implementations
Introduction, Number-Formats for Representation of Signals and Coefficients in DSP Structures, Dynamic Range and Precision, Sources of Errors in DSP Implementation, A/D Conversion Errors, DSP Computational Errors, D/A Conversion Error.

Unit 3
Architectures for Programmable Digital Signal Processing Devices
Introduction, Basic Architectural Features, Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

Unit 4
TMS320C5X Processor Architecture
Bus structure, Central Arithmetic Logic Unit, Auxiliary Register ALU, Index Register, Auxiliary Register Compare Register, Block Move Address Register, Block Repeat Registers, Parallel Logic Unit, Memory Mapped Register, Program Controller, Flags in Status Register, On-chip Memory, On-chip Peripherals, Assembly Language Syntax, Addressing Modes, Load/Store Instruction, Addition/ Subtraction Instruction, Move, Multiplication Instruction, NORM Instruction, Program Control Instruction, Peripheral Control.

Unit 5
TMS320C6X DSPs
Features Of TMS320C62X Processors, Internal Architecture, Central Processing Unit And Data Paths, Functional Units And Its Operations, Addressing Modes In C6X, Memory Architecture, External Memory Accesses, Pipeline Operation, and Peripherals.

Text Books
1. B. Venkata Ramani and M. Bhaskar, " Digital Signal Processors, Architecture, Programming" TMH, 2004.
2. Avtar Singh, S.Srinivasan, " DSP Implementation using DSP microprocessor with Examples from TMS32C54XX " Thamson 2004.
3. E.C.Ifeachor and B.W Jervis, "Digital Signal Processing a Practical approach," Pearson Publication.

Reference Books
1. Lapsley "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.
2. Jonathen Stein," Digital signal processing", John Wiley 2005.
3. S.K. Mitra," Digital Signal Processing", Tata McGraw-Hill Publication, 2001.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M. Tech I Sem.** Branch: **Electronics & Telecom.**
Subject: **RF circuit Design for Wireless Communication** Code: 528132 (28)
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in End Semester Exam. : **100**
Minimum number of class test to be conducted**: 02**

UNIT – I
Introduction to wireless circuit design
System Functions, the Radio Channel and Modulation Requirement, Analysis of Wireless System, Building Blocks, System Specifications, Testing.

UNIT – II
Models for Active Devices
Diodes, Bipolar Transistors, Field Effect Transistors, Parameter Extraction of Active Devices,

UNIT – III
Amplifier Design with BJT's And FET's
Properties of Amplifiers, Amplifier Gain, Stability and Matching, Single Stage Feedback Amplifiers, Two Stage Amplifiers, Differential Amplifiers, Biasing.

UNIT – IV
Mixer Design
Properties of Mixers, Diodes, Mixers, Transistor Mixers.

UNIT – V
RF/ Wireless Oscillators
Oscillator Design, Oscillator Circuit, Design of RF Oscillators, Noise in Oscillators, Reduction of Flicker Noise.

Text Book:
1. Ulrich L. Rohde "RF/microwave circuit design for wireless applications" John Wiley & Sons Publication.

References:
1. Inder bahl , " lumped elements for RF and microwave circuits", Artech house2003.
2. M. Kulkarni, " Microwave and Radar Engineering" Umesh Publication.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech I Sem** Branch: **Electronics & Telecom**
Subject: **Neural Network and Applications** Code: 528133 (28)
Total Theory Periods: **40** Total Tutorial Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02.**

Unit-I
Introduction to Neural Networks
Artificial Neural Networks: Basic Properties of Neurons, Biological Neurons & their artificial Models, Models of Artificial Networks, Neural Processing ,Learning & Adaptation, Learning, Neural Network Learning Rules.

Unit-II
Single Layer Perceptron Classifiers
Classification Model, Features And Decision Regions, Discriminant Functions, Linear Machine And Minimum Distance Classification, Nonparametric Training Concept, Training And Classification Using The Discrete Perceptron: Algorithm And Example; Single Layer Continuous Perceptron Networks for Linearly Separable Classifications. Multicategory Single Layer Perceptron Networks.

Unit-III
Multilayer Feed Forward Networks
Linearly Non separable Pattern Classification, Delta Learning Rule for Multiperceptron Layer, Generalized Delta Learning rule, Feed Forward Recall and Error Back Propagation Training; Examples of Error Back-Propagation. Training errors, Learning Factors: Initial weights, Cumulative Weight Adjustment versus Incremental Updating, Steepness of activation function, Learning Constant, Momentum Method, Network architecture Versus Data Representation, Necessary Number of Hidden Neurons.

Unit-IV
Single-Layer Feedback Networks
Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks, Mathematical Foundation of Gradient-Type Hopfield Networks. Transient Response of Continuous time Networks. Example Solution of Optimization Problems: Summing networks with digital output, Minimization of the Travelling salesman tour length.

Unit-V
Application Of Neural Algorithms And Systems
Linear Programmable Modelling Network, Character Recognition Networks: Multilayer Feed Forward Network For Printed Character Classification, Handwritten Digit Recognition: Problem Statement, Recognition Based On Handwritten Character Skeletonization, Recognition Of Handwritten Characters Based On Error, Back- Propagation Training. Neural Networks Control Applications: Overview Of Control Systems Concepts, Process Identification, Basic Nondynamic Learning Control Architectures, Inverted Pendulum Neurocontroller, Cerebellar Model Articulation Controller.

Text Books:
1. J.M.Zurada ," Introduction to Artificial Neural Systems", West Publishing Company.

Reference Books:
1. B. Yagananarayana, "Artificial Neural Networks", PHI, New Delhi.
2. Bose and Liang, "Artificial Neural Networks", Tata McGraw Hill, 1996.
3. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.
4. Kosco B, "Neural Networks and Fuzzy Systems: A Dynamic Approach to Machine Intelligence", Prentice Hall of India, New Delhi, 1992
5. Introduction Neural Networks Using MATLAB 6.0 - by S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Modern Digital Communication Lab** Code: 528121 (28)
Total Marks in End Semester Exam. : **75** Total Lab Periods: **40**

List of Experiments (to be performed at least 10 experiments)

1) Block Code For Erasure Correction In Network Communication Protocols.

2) Decoding of Convolution Encoded Bit Using Hard Decision Viterbe Decoding.

3) Encoding & Decoding of Reed-Solomon based Data Packets

4) Performing Normal/Shorted Reed Solomon Encoding for Code Word Length =255, Data Word Length=239.

5) Reed Solomon Encoding and Decoding by berlekemp massy algorithm.

6) Decoding of Turbo Code by Using BCJR Algorithm.

7) Compute the Distance Spectrum of a Turbo Code and the Union Bound on the BER

8) Simulate Program for Computation of the BER of an OFDM System With 16-QAM modulation.

9) Simulate the Performance of a Coding Scheme for Unequal Error Protection over an AWGN Channel.

10) TDMA (Time Divison Multiple Access) technique.

11) CDMA (Code Divison Multiple Access) technique.

12) Multipath Fading Channel.

Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)

Semester: **M.Tech. I Sem.** Branch: **Electronics &Telecom.**
Subject: **Simulation Lab with VHDL** Code: 528122 (28)
Total Practical Periods: **40**
Total Marks in End Semester Examination: **75**

List of Experiments (to be performed at least 10 experiments)

1) To design and simulate the basic gates.

2) Designing of the combinational blocks:

a) Mux b) Encoders c) Decoders

3) Designing and simulation of Code converters.

4) Designing, simulation and implementation 9-bit parity generator/checker.

5) Designing, simulation and implementation Flip-Flops.

6) Designing and simulation of Registers.

7) Designing and simulation of Counters.

8) FSM Modelling .

9) Designing, simulation and implementation of ROM.

10) Designing, simulation and implementation of RAM.

11) Designing, simulation and implementation of FIFO.

12) Design, simulation and implementation of ALU.

13) Designing and simulation of Filter.

14) Designing and simulation of FSK modulator and Demodulator.

15) Designing and simulation of PN generator.