CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Third Semester of B. Tech (IT) Examination
November- December 2015
IT217 Digital Logic & Design

Date: 30.11.2015, Monday   **Time: 10.00 a.m. To 01.00 p.m.**   **Maximum Marks: 70**

Instructions:
1. The question paper comprises two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

SECTION – I

Q - 1 **Answer the question below.**   **[07]**

a. Define Fan in.

b. Give the difference between PLA and PAL.

c. The voltages in digital electronics are continuously variable.

   a) True b) False

d. Which of the logic families listed below allows the highest operating frequency?

   a) TTL   b) ECL   c) HCMOS   d) 54S

e. The following waveform pattern is for _____.
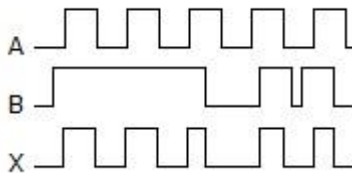
   a) 2-input AND gate

   b) 2-input OR gate

   c) Exclusive-OR gate

   d) None of the above

f. $(111111110010)_2 = ($_____$)_{16}$

g. Find 8's complement of $(346)_8$.

Q – 2.a 1) Subtract the following using 2's Complement   **[04]**

       i. 20 - 15

      ii. 10001 - 100001

   2) If $(302)_b / (20)_b = (12.1)_b$, then find the value of b.

Q – 2.b **Answer any two questions.** [10]

1) Design a combinational circuit that accept a three bit binary number and generate the binary equivalent of output multiply by 2 of input.

2) Design a 2 bit comparator circuit.

3) Design full subtractor combinational circuit.

Q - 3 **Answer the following.**

a. Obtain the set of prime implicants for the Boolean expression [06]

$$f = \sum m(0, 1, 6, 7, 8, 9, 13, 14, 15) \text{ using tabulation method.}$$

b. 1. Implement the following function using multiplexer, [04]

$$F(a,b,c) = \sum m (1, 3, 5, 6). \text{ Choose 'a' and 'b' as select line.}$$

2. Simplify the following function using Boolean algebra.

[04]

    i. X'Y'+ XY + X'Y

    ii. A + B + A'B'C

OR

1. Implement following function with 3 to 8 decoder and NOR gate.

[04]

    i. F(a, b, c) = $\sum m$ (0,1,2,4,6).

    ii. F(x, y, z) = X' + Y'Z

2. A digital circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. by mean of a truth table, find the Boolean function for three bit input. [04]

SECTION – II

Q - 4 **Answer the question below.** [07]

a. Give the difference between ROM and RAM.

b. One example of the use of an S-R flip-flop is as a _____.

a) Racer

b) Astable Multivibrator

c) Binary storage element

d) Transition pulse generator

c. The storage element for a static RAM is the _____.

a) Diode   b) Register   c) Capacitor   d) Flip-flop.

d. On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.

a) Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0

b) Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0

c) Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1

d) Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1

e. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

a) 0000   b) 0010   c) 1000   d) 1111

f. What is the disadvantage of R S flip flop?

g. Write down a Excitation table and State table for S R flip flop.

Q – 5.a Design BCD to Excess-3 code converter. **[05]**

OR

Q – 5.a Express the given Boolean function in sum of minterm and convert to other canonical **[05]** form. Also obtain complement of given function using duality principle.

$$F(x,y,z) = X'Z' + X(Y'Z' + YZ)$$

Q – 5.b Draw the Johnson counter which can generate 6 different timing signal . Also mention **[04]** the timing sequence with respective required decoding.

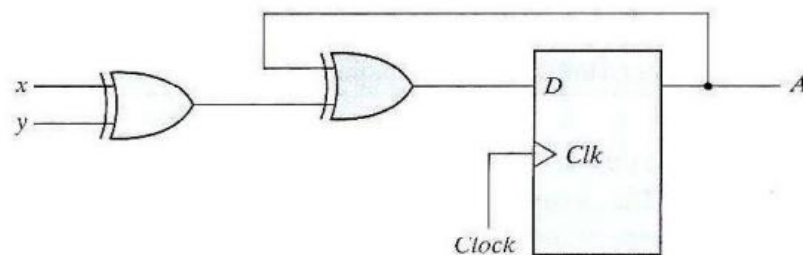**Q – 5.c** Derive a state table , state diagram and state equation for the given sequential circuit in **[05]** Figure 1.

Figure 1.

OR

Q – 5.c   Apply state reduction algorithm for the sequential circuit given in Figure 2.   **[05]**
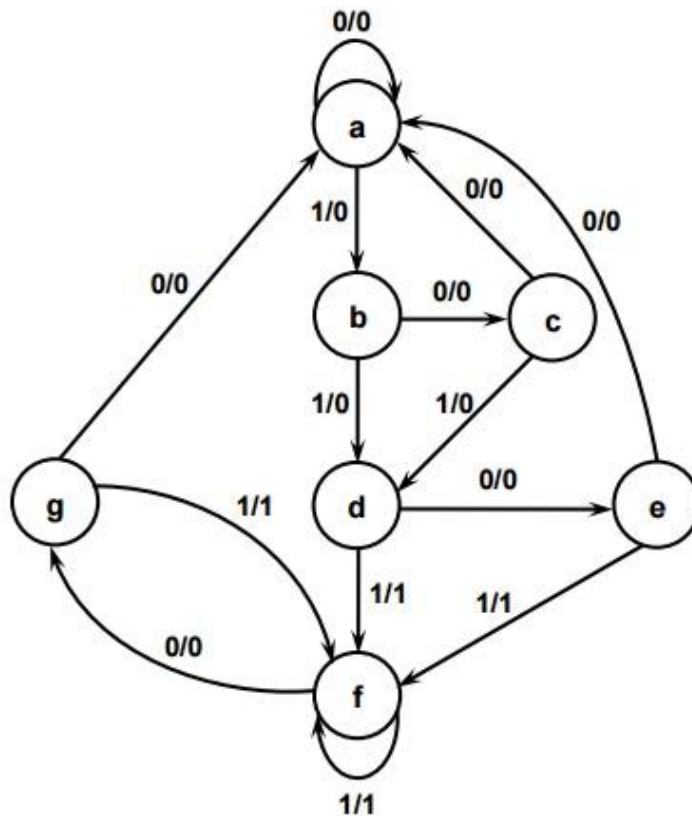

Figure 2.

Q – 6.a   Give the importance of master slave Flip flop and draw logic diagram of master slave   **[03]**
J-K flip flop.

Q – 6.b   Design a mod -11 down counter using J K flip flop.   **[07]**

Q – 6.c   Draw and explain 4 bit binary ripple counter.   **[04]**

OR

Q – 6.a   Design a counter with the following binary sequence: 0,1,3,7,6,4 and repeat. Use T flip   **[07]**
flop.

Q – 6.b   Explain 2 bit universal shift .   **[04]**

Q – 6.c   Give the difference between synchronous and asynchronous circuits.   **[03]**

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