

# CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

II Semester of MSc (Physics) Examination May 2018

Course code & Name PS721 ELECTRONICS

Date: 03/05/2018 Day: Thursday Time: 1.30 pm To 2.00 pm Maximum Marks: 20

## MCQ

### Important Instructions:

- Tick the correct answer and it should be written in question paper itself.
- Use of non-programmable calculator is allowed.

**Q - I Write the correct answer for the following questions. (One mark each) 20**

1. When an op amp is not saturated, the voltages at the non-inverting and inverting inputs are
  - (i) Almost zero
  - (ii) Much different
  - (iii) Equal to the output voltage
  - (iv) Equal to  $\pm 15$  V
2. An ideal op amp
  - (i) has always sine waves as signals
  - (ii) does not go into saturation
  - (iii) has constant gain bandwidth product
  - (iv) has infinite input impedance and zero output impedance
3. In a controlled current source with op amps, the circuit acts like
  - (i) Voltage amplifier
  - (ii) Current –to- voltage converter
  - (iii) Voltage –to- current converter
  - (iv) Current amplifier
4. Negative feedback does not improve
  - (i) Stability of voltage gain
  - (ii) Nonlinear distortion in later stage
  - (iii) Output offset voltage
  - (iv) Power bandwidth

5. In an averaging circuit, the input resistances are
  - (i) Equal to feedback resistance
  - (ii) Less than the feedback resistance
  - (iii) Greater than the feedback resistance
  - (iv) Unequal
6. A memory cell that represents result of a latch can store \_\_\_\_\_.
  - (i) 1 bit
  - (ii) 1 byte
  - (iii) 4 bit
  - (iv) 4 byte
7. System having memory elements are called
  - (i) combinational circuits
  - (ii) sequential circuits
  - (iii) logic circuits
  - (iv) complex circuits
8. A D/A converter is an application of the
  - (i) Adjustable bandwidth circuit
  - (ii) Non-inverting amplifier
  - (iii) Voltage to current converter
  - (iv) Summing amplifier
9. The IC series \_\_\_\_\_ is used as positive voltage regulators, while \_\_\_\_\_ is used as negative voltage regulators. (Fill in the blank)
10. Single-bit indicators that may be set or cleared to show the results of logical or arithmetic operations are the:
  - (i) flags
  - (ii) registers
  - (iii) monitors
  - (iv) decisions
11. The bit sequence 0101 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
  - (i) 0101
  - (ii) 1010
  - (iii) 0110
  - (iv) 0100
12. An oscillator always needs an amplifier with
  - (i) Positive feedback
  - (ii) Negative feedback
  - (iii) Compensating capacitors
  - (iv) Pullup resistors
13. If bandwidth increases,
  - (i) The center frequency decreases
  - (ii) Q decreases
  - (iii) The roll-off rate increases
  - (iv) Ripples appear in the stopband
14. Feedback among logic gates make asynchronous system
  - (i) stable
  - (ii) unstable
  - (iii) complex
  - (iv) combinational
15. A counter that flows binary sequence is called
  - (i) ripple counter
  - (ii) edge counter
  - (iii) binary counter
  - (iv) level counter

16. In the world of microprocessor, a combination of letters to suggest the operation of an instruction is known as \_\_\_\_\_.
- (i) ASCII code (ii) Compiler  
(iii) Machine code (iv) Mnemonics
17. A shift register that accepts a parallel input, or a bidirectional serial load and internal shift features is known as \_\_\_\_\_ shift register.
- (i) Tristate (ii) End around  
(iii) Universal (iv) conversion
18. State of flipflop can be switched by changing its
- (i) input signal (ii) output signal  
(iii) momentary signals (iv) all signals
19. One multiplexer can take the place of \_\_\_\_\_
- (i) several SSI logic gates (ii) combinational logic circuits  
(iii) several Ex-NOR gates (iv) several SSI logic gates or combinational logic circuits
20. Which digital system translates coded characters into a more useful form?
- (i) Encoder (ii) Display  
(iii) Counter (iv) Decoder

# CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

II Semester of MSc (Physics) Examination May 2018

Course code & Name PS721 ELECTRONICS

Date: 03/05/2018 Day: Thursday Time: 2.00 pm To 4.30 pm Maximum Marks: 50

## Instructions:

1. Section I and II must be attempted in TWO ANSWER SHEET.
2. Make suitable assumptions and draw neat figures wherever required.
3. Use of non-programmable calculator is allowed.
4. Show necessary calculations.

## SECTION -I

Q – II Answer the following questions as directed

1 Attempt any Two. (Four marks each)

[8]

- (a) (i) Describe the ideal characteristics of an ideal op-amp.
- (ii) Determine the bandwidth of an AC inverting amplifier. Given,  $R_{in} = 50 \Omega$ ,  $C_i = 0.1 \mu F$ ,  $R_1 = 100 \Omega$ ,  $R_F = 1 k\Omega$ , and supply voltage  $= \pm 15 V$ .
- (b) (i) Briefly explain the need for compensating networks in op-amps.
- (ii) Calculate the open-loop voltage gain as a function of frequency at  $f = 0$  MHz and  $f = 1$  MHz. For an op-amp 741C, the values of gain and break frequency are respectively  $2 \times 10^5$  and 5 Hz.
- (c) (i) Briefly explain the differences between the two operating modes of the 555 timer.
- (ii) What must the relationship between the pulse width  $t_p$  and the period  $T$  of the input trigger signal if the 555 is to be used as a divide-by-2-network?

2 Solve any Four. (Three marks each)

[12]

- (a) For the non-inverting amplifier with compensative network circuit,  $R_{in} = 50 \Omega$ ,  $C_i = C_1 = 0.1 \mu F$ ,  $R_1 = R_2 = 100 k\Omega$ ,  $R_F = 1 M\Omega$ , and  $V_{CC} = 15 V$ . Determine (a) the bandwidth of the amplifier and (b) the maximum output voltage swing.
- (b) The 741C is used for the differential amplifier with single op-amp  $R_1 = R_2 = 100 \Omega$  and  $R_F = R_3 = 3.9 k\Omega$ . Other specifications provided are:  $A = 2,00,000$ ,  $R_i = 2 M\Omega$ ,  $R_o = 75 \Omega$ ,  $f_o = 5$  Hz, and  $UGB = 1$  MHz, supply voltages  $= \pm 15 V$ , Maximum output voltage swing  $= \pm 13 V$ . Calculate the close-loop voltage gain, and calculate the input resistances  $R_{iF_x}$  and  $R_{iF_y}$  assuming that the circuit is initially nulled.
- (c) Design a wide band-pass filter with  $f_L = 200$  Hz,  $f_H = 1$  kHz and a passband gain  $= 4$ . Draw the frequency response plot of this filter. Calculate the value of  $Q$  for the filter.
- (d) A non-inverting averaging amplifier with the following specifications:  $V_a = V_b = 1.5 V$ ,  $V_c = 3 V$ ,  $R_1 = R = 1.5 k\Omega$ , and  $V_o = 5.2 V$ . Determine the required value of  $R_F$ .
- (e) What is a voltage regulator? List four different types of voltage regulators.

## SECTION - II

### Q-III Answer the following questions as directed

#### 1. Attempt any Three. (Six marks each)

[18]

(a) Prove following expressions using De Morgan's theorem.

(i)  $AB + \overline{AC} + A\overline{B}C(AB + C) = 1$

(ii)  $AB + A\overline{B}C + B\overline{C} = AC + B\overline{C}$

(iii)  $A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$

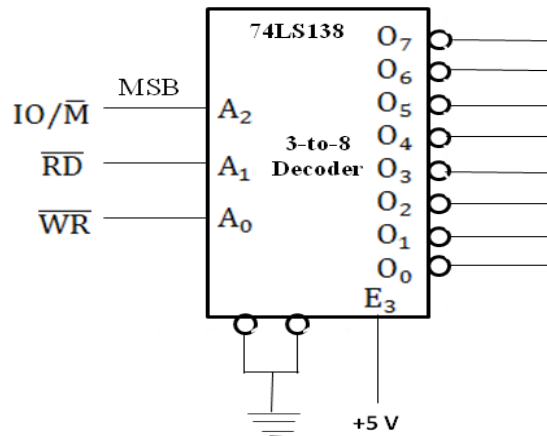
(b) (i) Distinguish between synchronous and asynchronous latches.

(ii) Design mod-9 synchronous counter using J-K FFs.

(c) (i) For the 4-bit weighted-resistor DAC, determine (a) the weight of each input bit if the inputs are 0 V and 5 V, (b) the full scale output, if  $R_f = R = 1 \text{ k}\Omega$ . Also find the full-scale output if  $R_f$  is changed to  $500 \Omega$ .

(ii) Describe the advantages of the R-2R ladder DAC over the weighted-resistor type DAC.

(d) (i) Explain why four output signals are invalid or meaningless in the following figure.



(ii) Explain the functions of the ALE and  $\text{IO}/\overline{\text{M}}$  signals of the 8085 microprocessor.

#### 2. Attempt any Four. (Three marks each)

[12]

(a) Reduce following expressions using De Morgan's theorem.

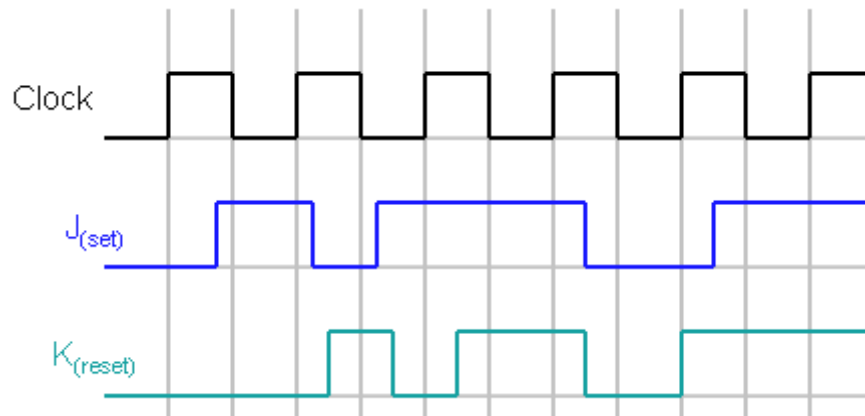
(i)  $\overline{\overline{(A + B)(C + D)} \overline{(E + F)(G + H)}}$

(ii)  $\overline{(P + Q)(R + S)}$

(iii)  $A + \overline{BC}(A + \overline{BC})$

(b) What is a master-slave flip-flop? Draw its circuit diagram and discuss its working function using truth table and waveforms.

- (c) What are the various types of shift-registers? Explain anyone with circuit diagram and truth table.
- (d) Assume register B holds 93H and accumulator holds 15H. Illustrate the results of the instructions ORA B, XRA B, and CMA.
- (e) The waveform shown in below figure is applied to negative edge triggered J-K FF. Draw and explain the output waveform  $Q$  and  $\bar{Q}$  along with the truth table.



- (f) Describe the operations performed by
- Half-adder
  - Half-subtractor